Operating System Practice

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Grading

▸ Midterm: 20%

▸ Lab Exercises: ~~20%~~ ➜ 10%

   ◦ Homework: 10%

   ◦ Labs: N/A

▸ Quizzes and Attendance: ~~20%~~ ➜ 26%

   ◦ Quizzes 1, 2: 8%, 8%

   ◦ Attendance: 10%

▸ Final Exam: ~~20%~~ ➜ 22%

▸ Final Project: ~~20%~~ ➜ 22%

Flash Memory and Phase Change Memory

Reference: Prof. Tei-Wei Kuo, NTU and Dr. Yuan-Hao Chang, Academia Sinica

Trends – Market and Technology

▸ Diversified Application Domains
  ◦ Portable Storage Devices
  ◦ Consumer Electronics
  ◦ Industrial Applications
▸ Competitiveness in the Price
  ◦ Dropping Rate and the Price Gap with HDDs
▸ Technology Trend over the Market
  ◦ Improved density
  ◦ Degraded performance
  ◦ Degraded reliability

Trends – Storage Media

2,000,000 Miles Per Hour

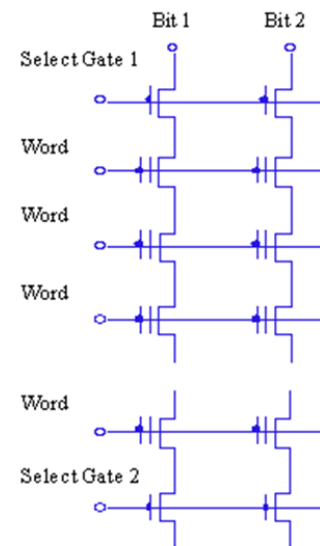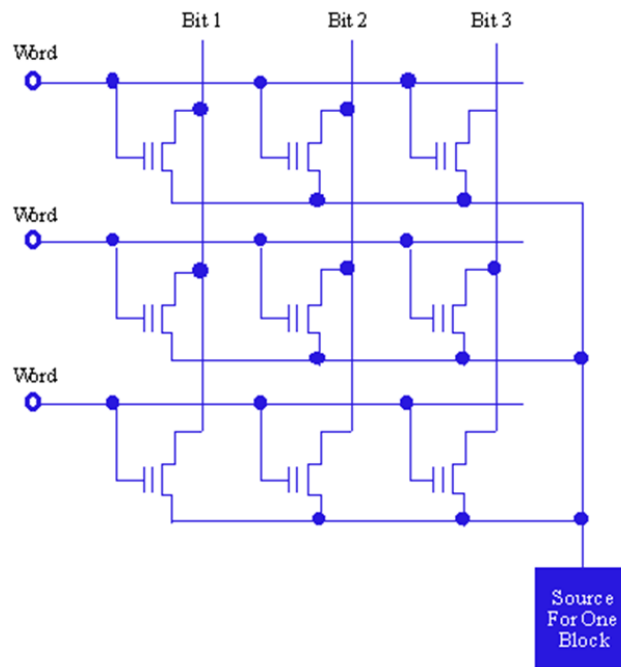*Fly By Night*

Boeing 747

1/100" Flying Height
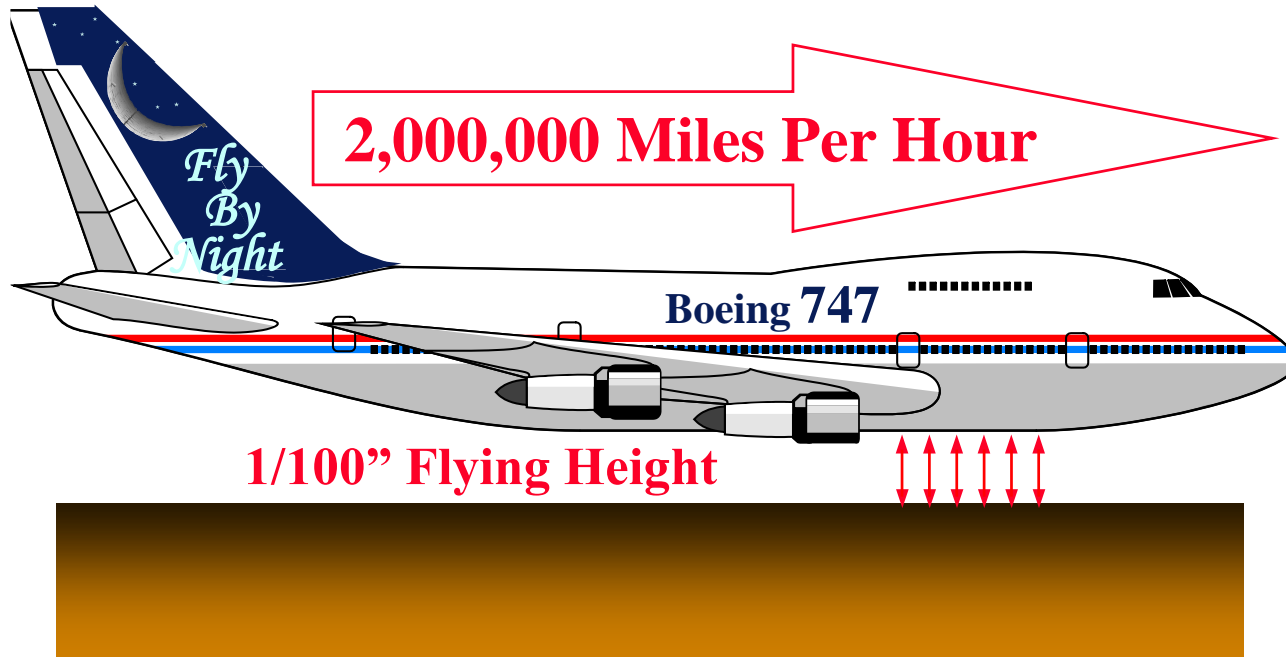
VS

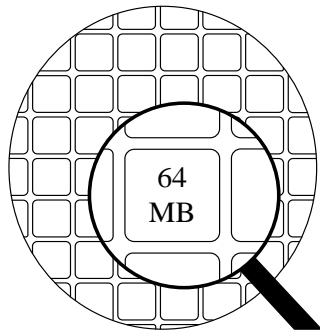Source: Richard Lary, The New Storage Landscape: Forces shaping the storage economy, 2003.

NOR and NAND Flash

▸ NAND accesses each cell through adjacent cells, while NOR allows for individual access to each cell

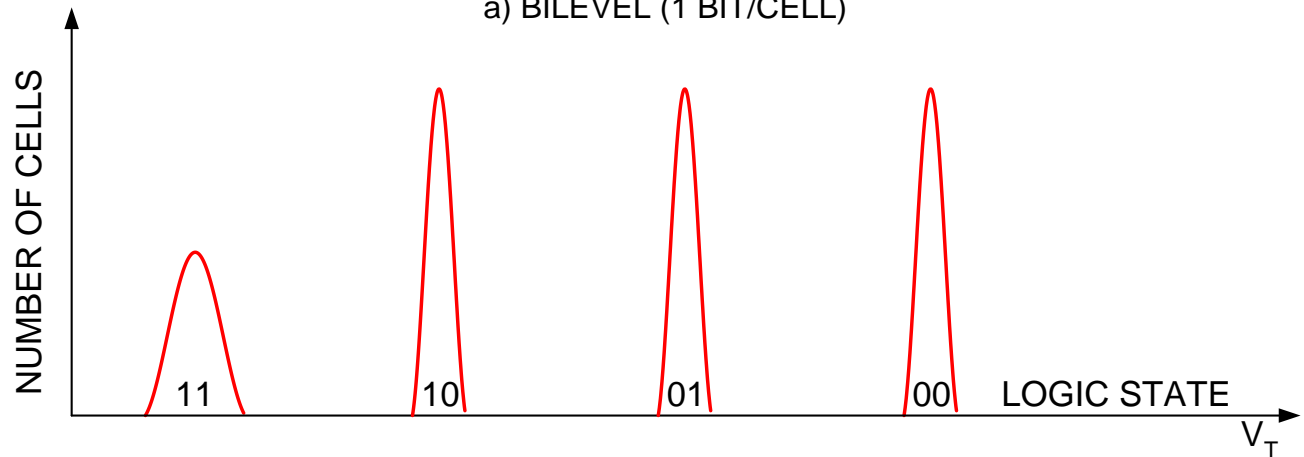▸ The cell size of NAND is almost half the size of a NOR cell

Single-Level Cell (SLC) vs Multi-Level Cell (MLC) Flash

SLC Flash

MLC Flash

a) BILEVEL (1 BIT/CELL)
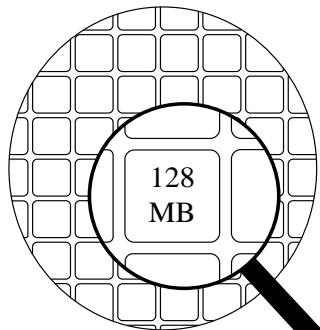
b) MULTILEVEL (2 BIT/CELL)

System Architectures for Flash Management
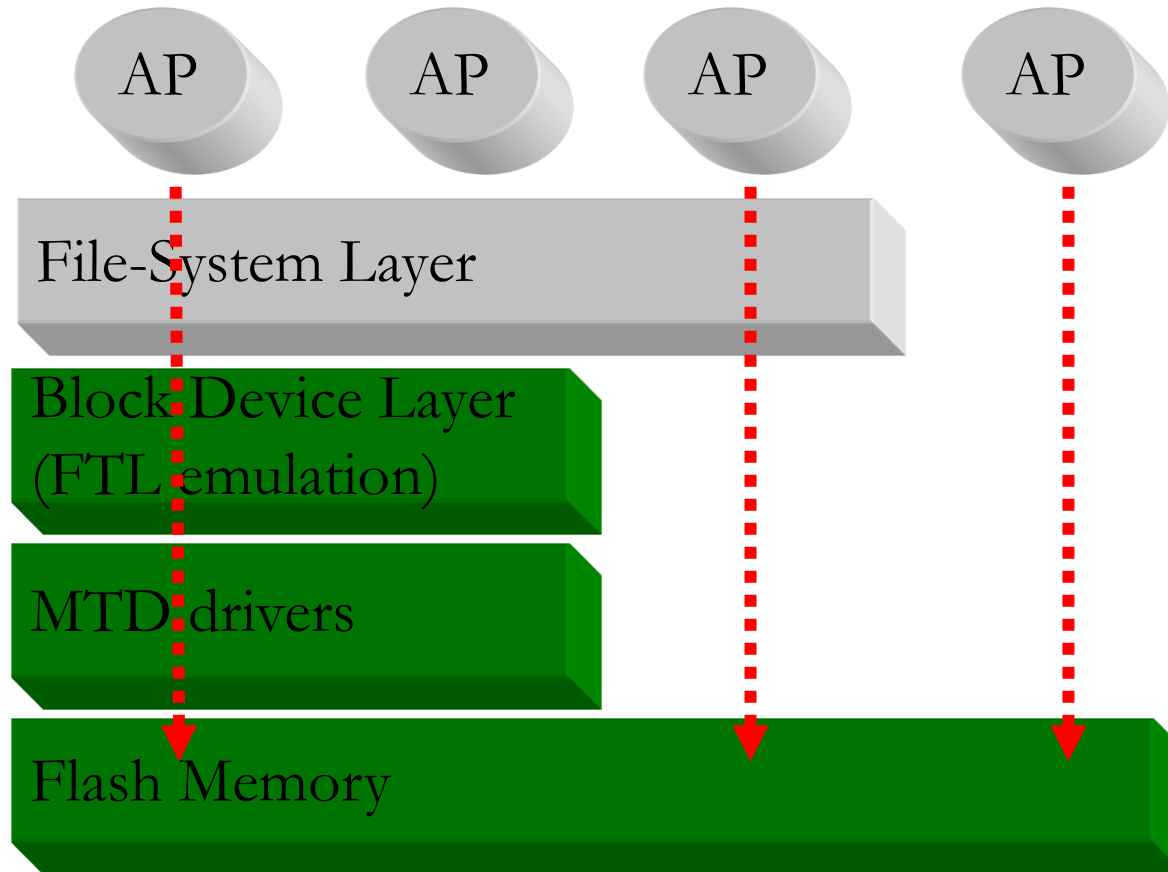
Flash-Memory Characteristics

▸ Write-Once
  ◦ No writing on the same page unless its residing block is erased
  ◦ Pages are classified into valid, invalid, and free pages

▸ Bulk-Erasing
  ◦ Pages are erased in a block unit to recycle used but invalid pages

▸ Wear-Leveling
  ◦ Each block has a limited lifetime in erasing counts

Page Write and Block Erase

Write one page

1 Page = 512B—4KB
1 Block = 32 pages

Block 0

Block 1

Block 2

Block 3

Erase one block

Out-Place Update

A	B	C	D								
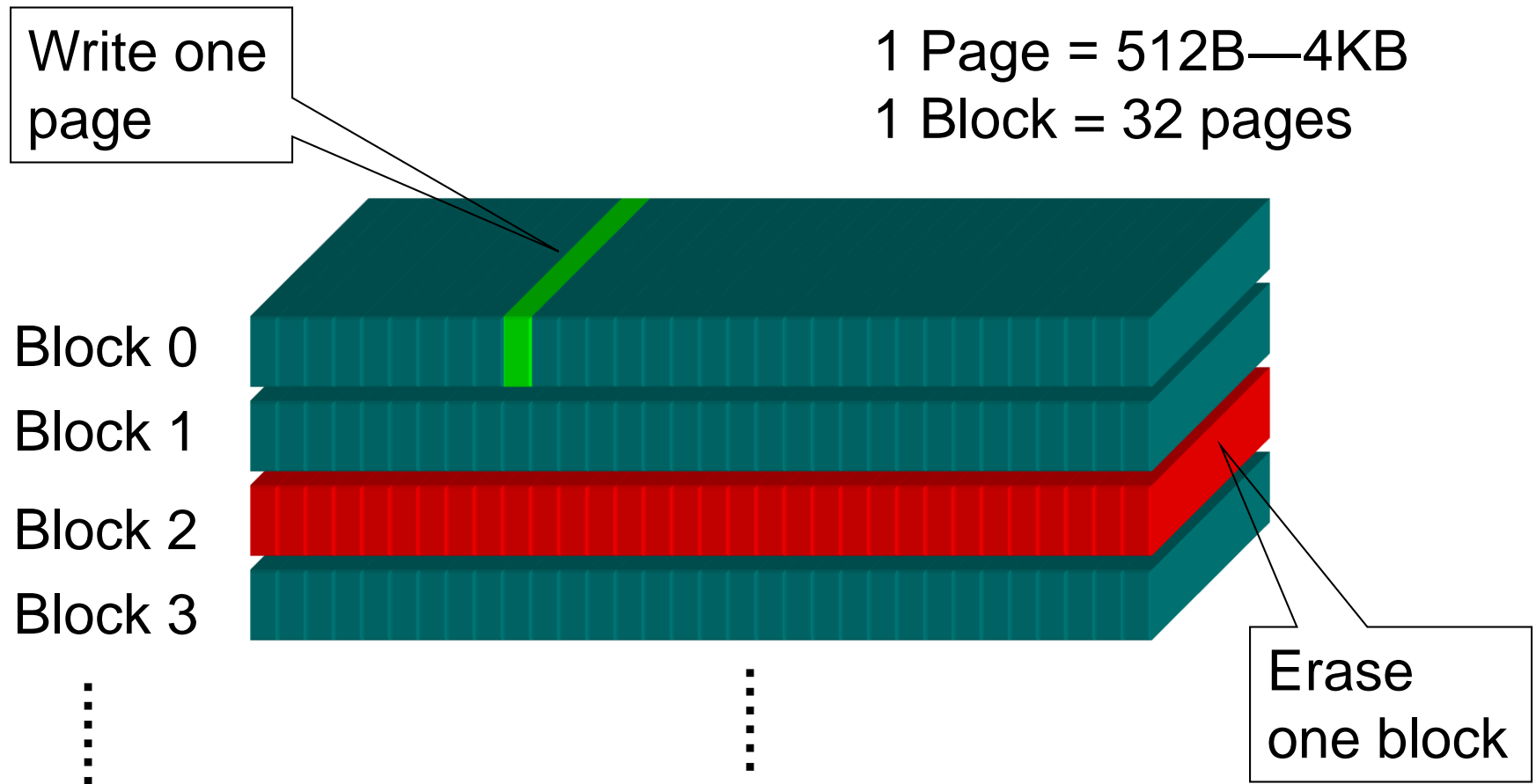
Live pages   Free pages
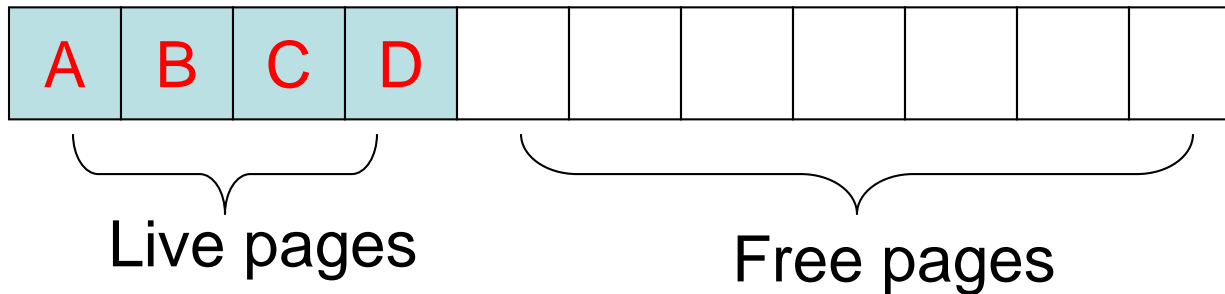
Suppose that we want to update data A and B…

A	B	C	D		A			B		
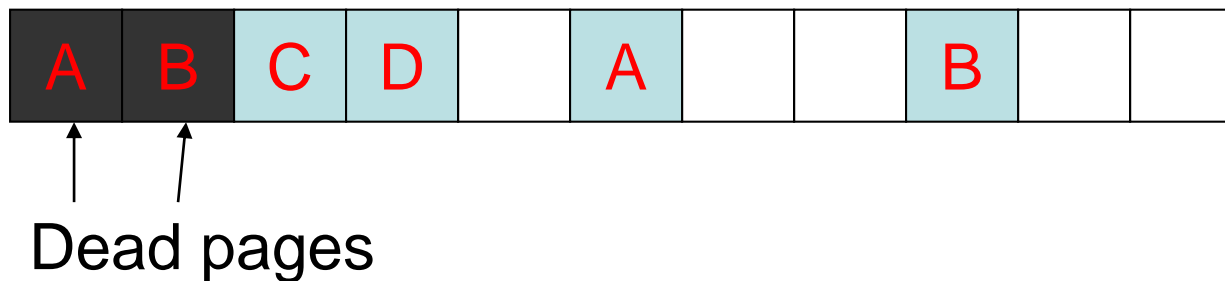
Dead pages

Garbage Collection (1 /3)

L	D	D	L	D	D	L	D

← This block is to be recycled
(3 live pages and 5 dead pages)

L	L	D	L	L	L	F	D

L	F	L	L	L	L	D	F

F	L	L	F	L	L	F	D

■ A live page
■ A dead page
□ A free page

Garbage Collection (2/3)
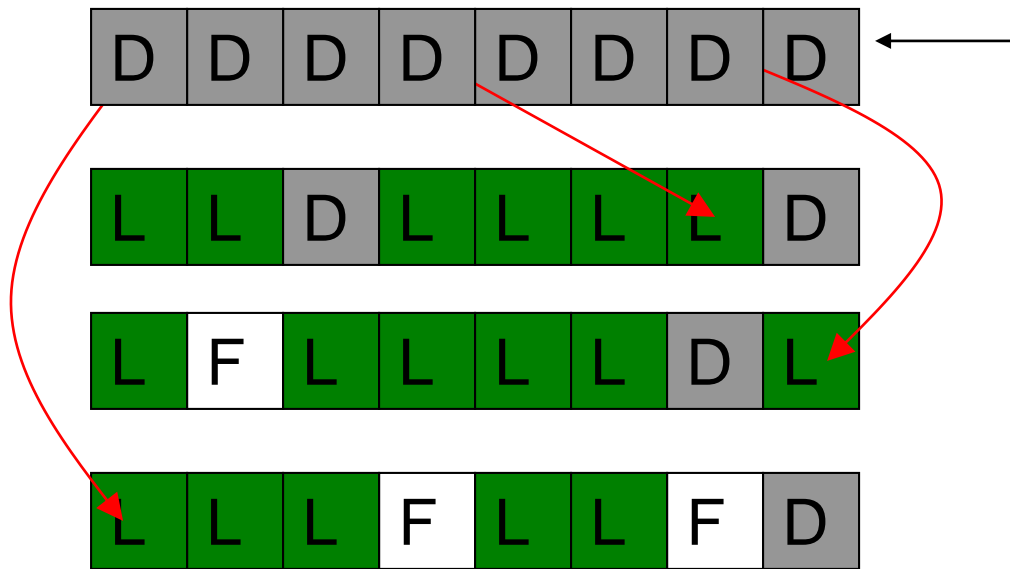
Live data are copied to somewhere else

- 🟩 A live page
- ⬜(gray) A dead page
- ☐ A free page

Garbage Collection (3/3)

F	F	F	F	F	F	F	F

The block is then erased

L	L	D	L	L	L	L	D

Overheads:
- live data copying
- block erasing

L	F	L	L	L	L	D	L

L	L	L	F	L	L	F	D

■ A live page
■ A dead page
□ A free page

Wear-Leveling
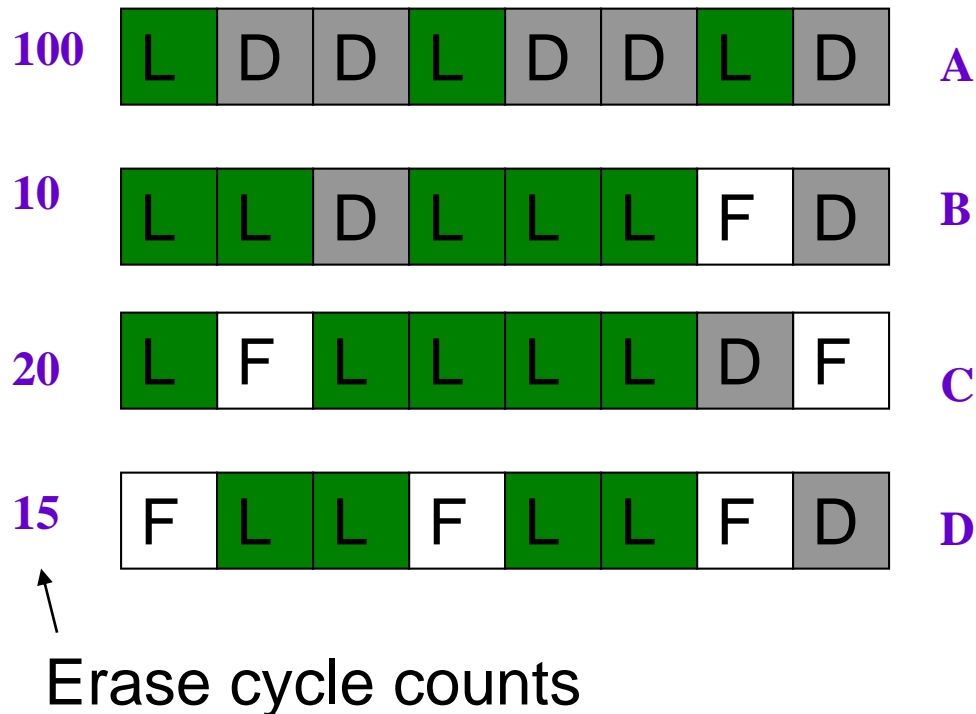
Wear-leveling might interfere with the decisions of the block-recycling policy

100	L	D	D	L	D	D	L	D	A
10	L	L	D	L	L	L	F	D	B
20	L	F	L	L	L	L	D	F	C
15	F	L	L	F	L	L	F	D	D

Erase cycle counts

🟩 A live page
⬜(gray) A dead page
☐ A free page

Flash Translation Layer

xD,
SmartMedia

SD,
Memory Stick,
Compact Flash

Host

| Applications |
| Operating System |
| File System (e.g. DOS FAT) |
| FTL |
| MTD |

Device

| Flash Media |

Host

| Applications |
| Operating System |
| File System (e.g. DOS FAT) |

Device

| FTL |
| MTD |
| Flash Media |
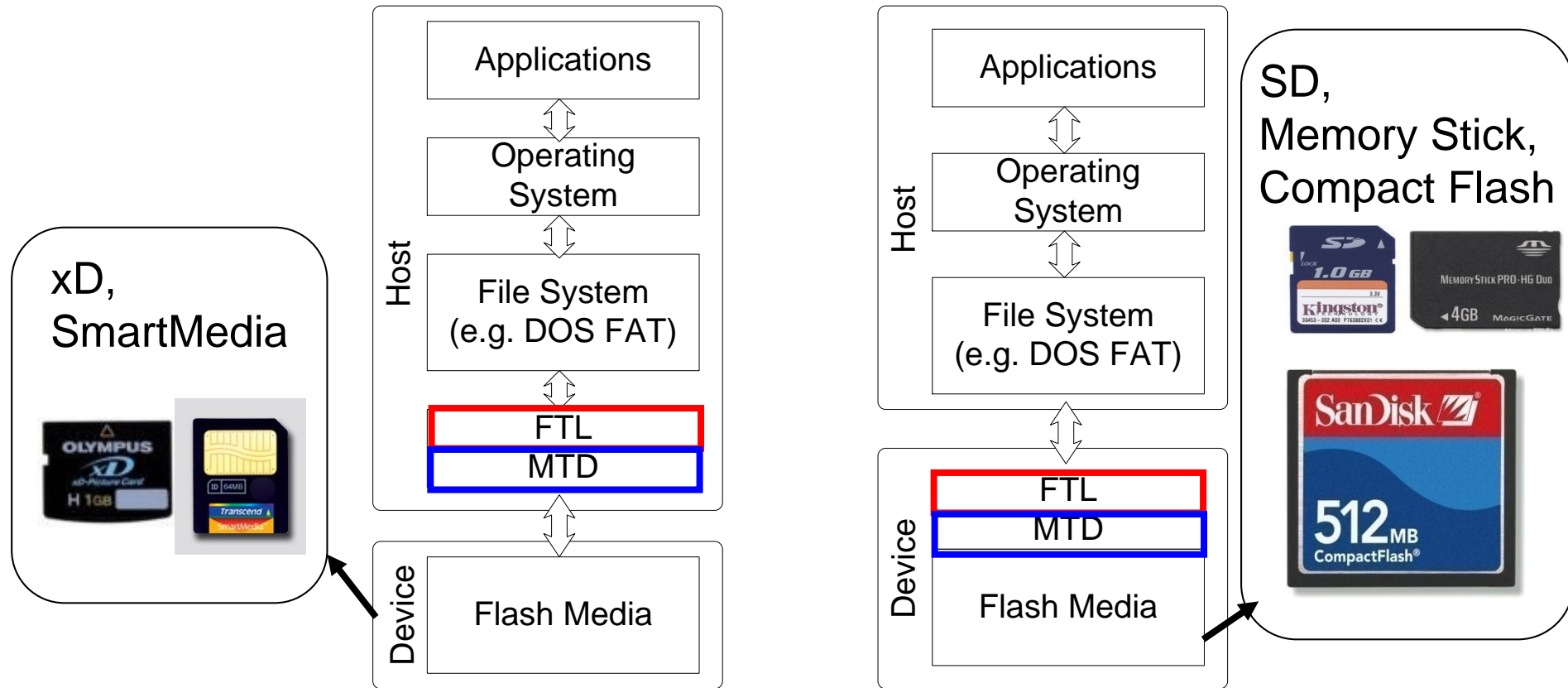
*FTL: Flash Translation Layer, MTD: Memory Technology Device

Policies – FTL

▸ FTL adopts a page-level address translation mechanism

Policies – NFTL (Type 1)

- A logical address under NFTL is divided into a virtual block address and a block offset, e.g., LBA=1011 => virtual block address (VBA) = 1011 / 8 = 126 and block offset = 1011 % 8 = 3

NFTL Address Translation Table (in main-memory)

A Chain Block
Address = 9

A Chain Block
Address = 23

A Chain Block
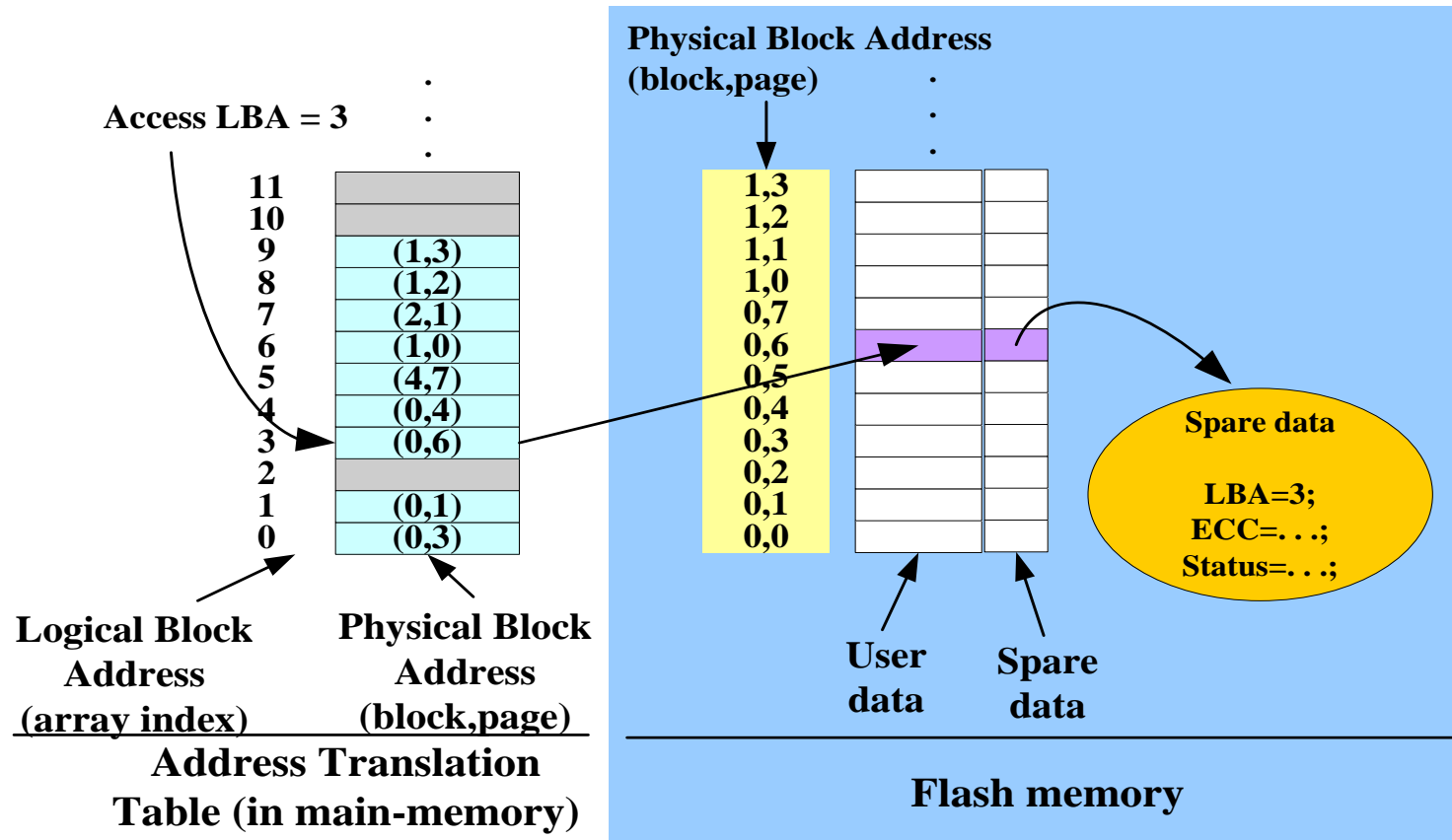Address = 50

Write data to LBA=1011

(9)

VBA=126

Block Offset=3

Free	Free	Free
Free	Free	Free
Free	Free	Free
Used	Used	Free
		Free
		Free
		Free
		Free

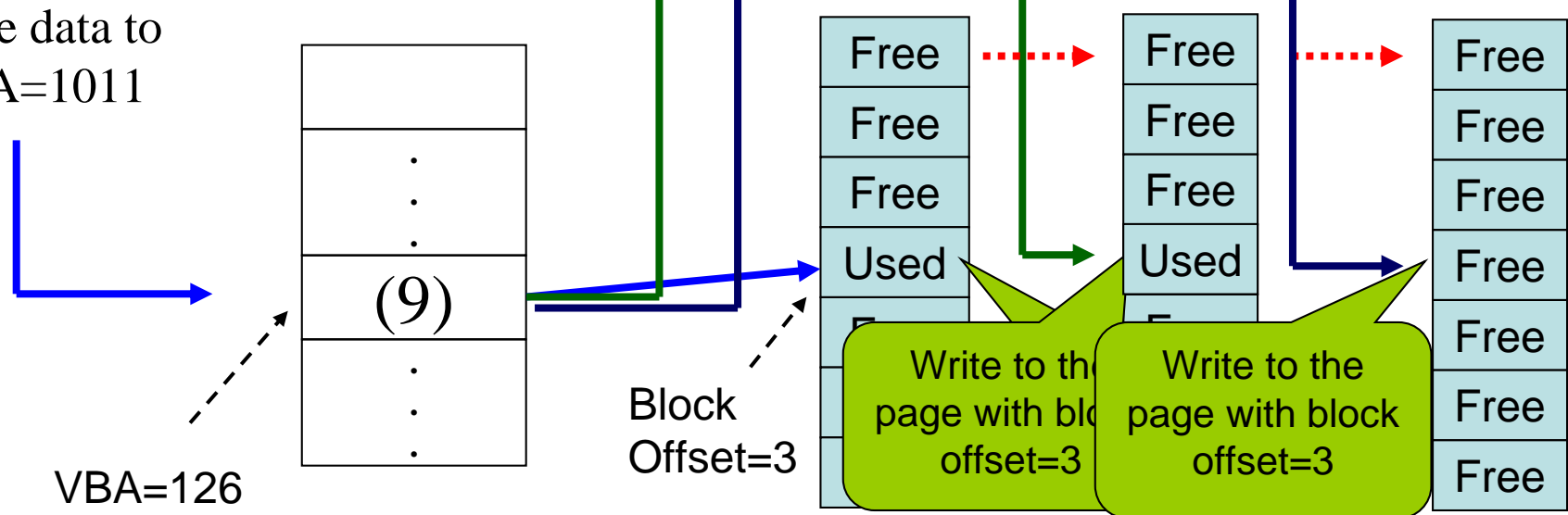Write to the page with block offset=3

Write to the page with block offset=3

Policies – NFTL (Type 2)

▸ A logical address under NFTL is divided into a virtual block address and a block offset, e.g., LBA=1011 => virtual block address (VBA) = 1011 / 8 = 126 and block offset = 1011 % 8 = 3

NFTL Address Translation Table (in main-memory)

A Primary Block
Address = 9

A Replacement Block
Address = 23

Write data to LBA=1011

(9,23)

VBA=126

Block Offset=3

Primary Block	Replacement Block
Free	Used
Free	Used
Free	Used
Used	Free
Free	

Write to the first free page

the page has been ...ed

Free
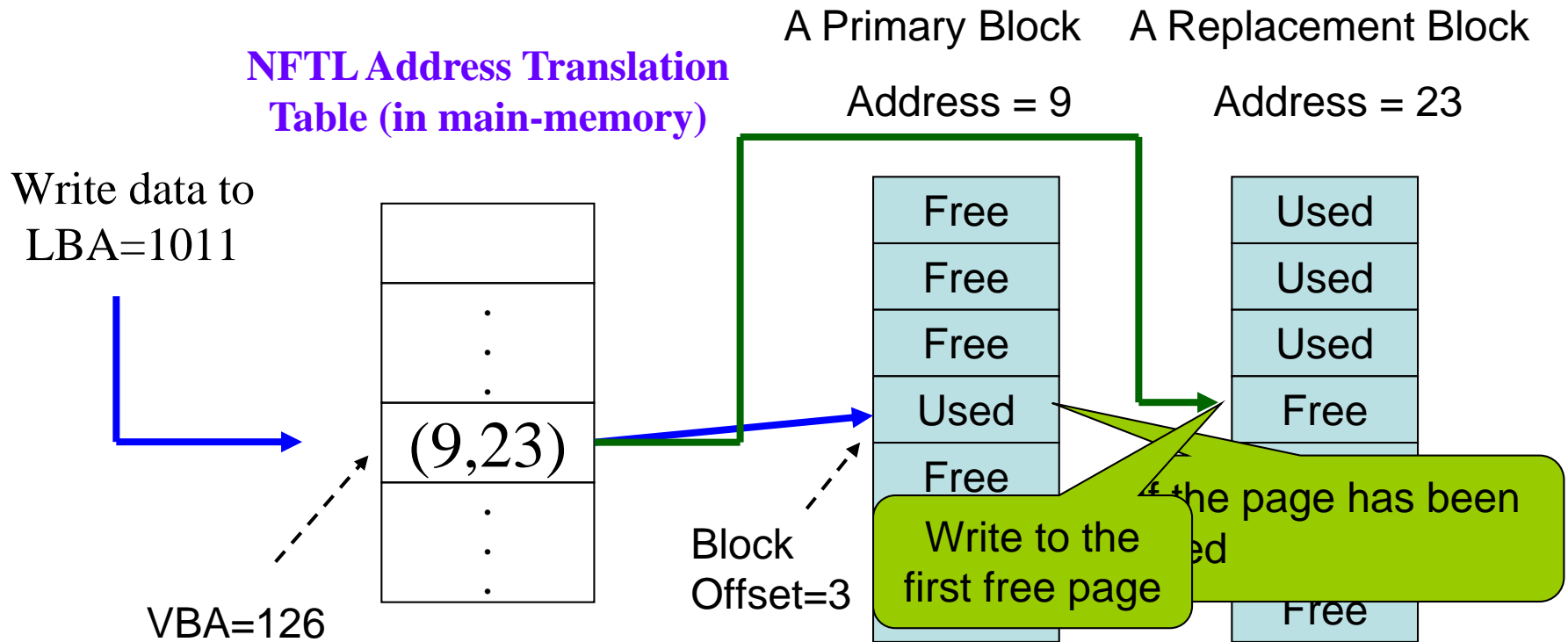
Challenges and Research Topics of Flash Memory Designs

- Performance
    - Reduce the overheads of Flash management
    - Reduce the access time to data
    - Reduce the garbage collection time
- Reliability
    - Error correcting codes
    - Log systems
- Endurance
    - Dynamic wear-leveling
    - Static wear-leveling

3D Flash Memory

▸ 3D flash memory provides a good chance to further scale down the feature size and to reduce the bit cost.
  ◦ Deliver very large storage space
  ◦ Worsen program disturbance
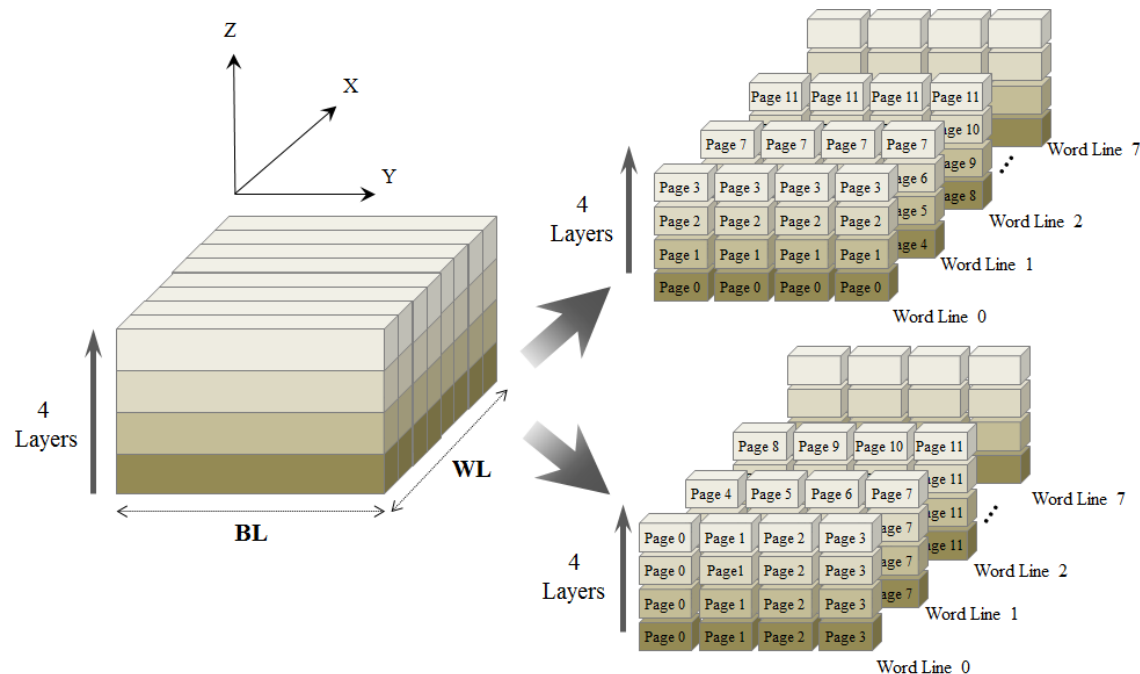
Deteriorated Disturb on 3D Flash

Z

X

Y

4 Layers

BL

WL

4 Layers

Page 4	Page 4	Page 4	Page 4	Word Line 7
Page 3	Page 3	Page 3	Page 3	Word Line 6
Page 2	Page 2	Page 2	Page 2	Word Line 5
Page 1	Page 1	Page 1	Page 1	Word Line 4

Word Line 3
Word Line 2
Word Line 1
Word Line 0

Type H

█ Programmed Page

█ Disturbed Page

4 Layers

Page 1	Page 2	Page 3	Page 4	Word Line 7
Page 1	Page 2	Page 3	Page 4	Word Line 6
Page 1	Page 2	Page 3	Page 4	Word Line 5
Page 1	Page 2	Page 3	Page 4	Word Line 4

Word Line 3
Word Line 2
Word Line 1
Word Line 0

Type V