

Operating System Practice

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Flash Memory and Phase Change Memory

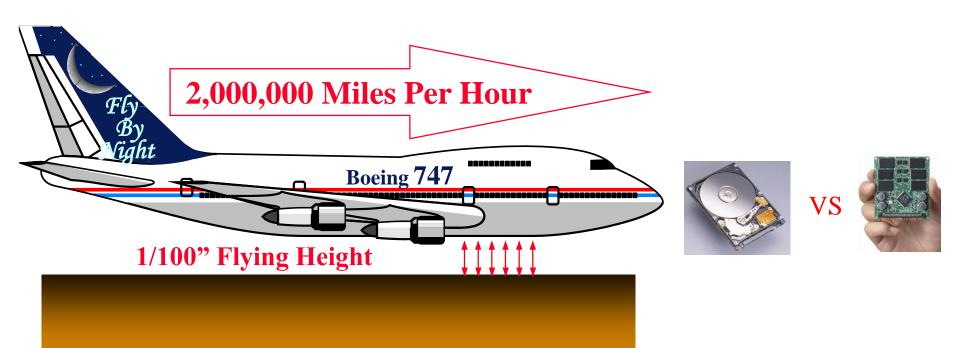
Reference: Prof. Tei-Wei Kuo, NTU and Dr. Yuan-Hao Chang, Academia Sinica

Trends - Market and Technology

- Diversified Application Domains
 - Portable Storage Devices
 - Consumer Electronics
 - Industrial Applications
- Competitiveness in the Price
 - Dropping Rate and the Price Gap with HDDs
- Technology Trend over the Market
 - Improved density
 - Degraded performance
 - Degraded reliability



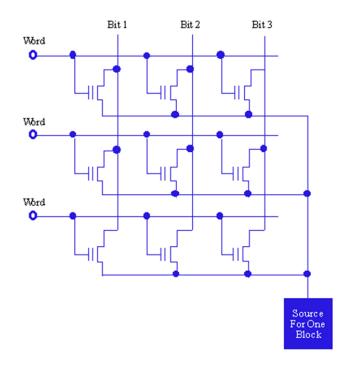
Trends - Storage Media

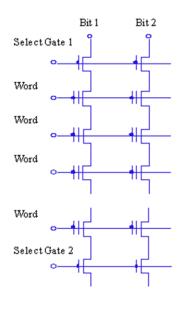


Source: Richard Lary, The New Storage Landscape: Forces shaping the storage economy, 2003.

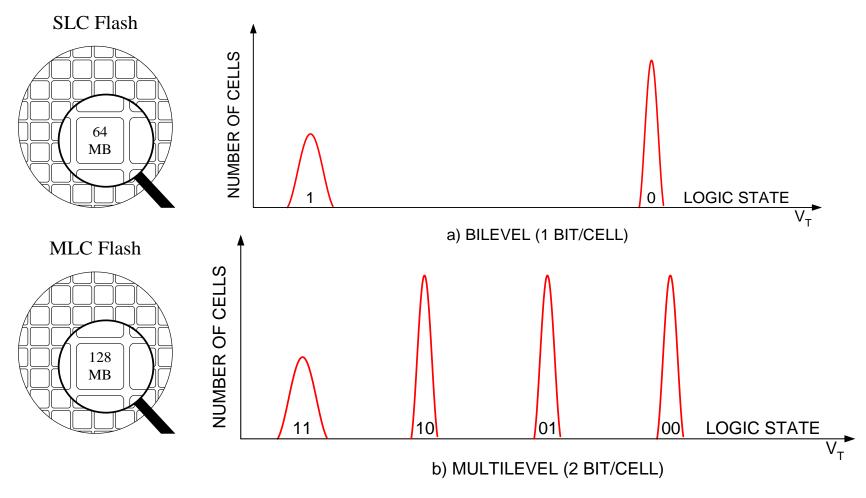
NOR and NAND Flash

- NAND accesses each cell through adjacent cells, while NOR allows for individual access to each cell
- ▶ The cell size of NAND is almost half the size of a NOR cell

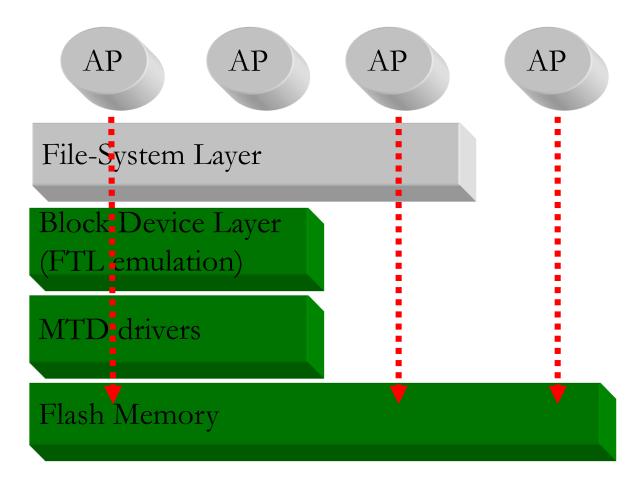




Single-Level Cell (SLC) vs Multi-Level Cell (MLC) Flash



System Architectures for Flash Management

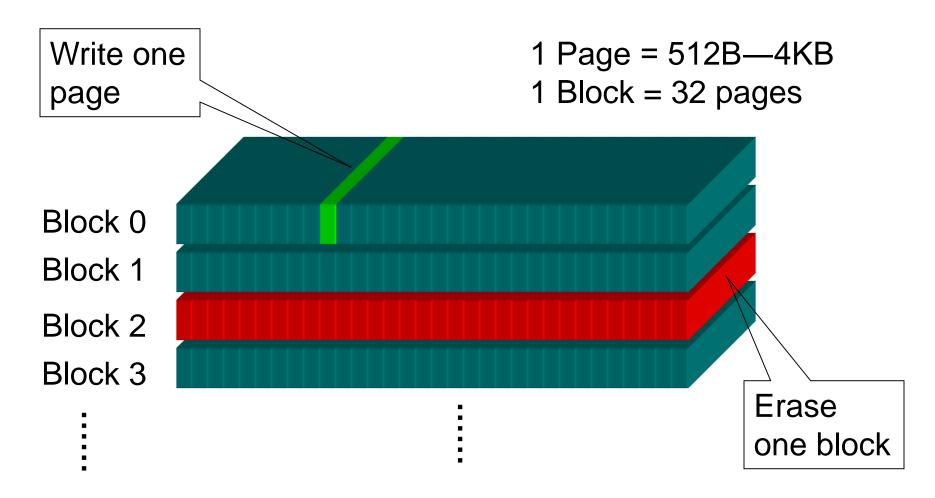


Flash-Memory Characteristics

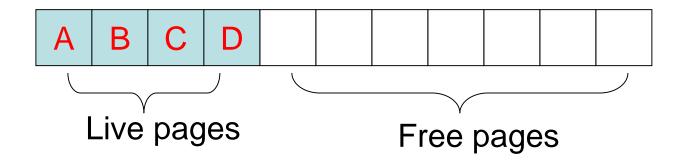
- Write-Once
 - No writing on the same page unless its residing block is erased
 - Pages are classified into valid, invalid, and free pages
- Bulk-Erasing
 - Pages are erased in a block unit to recycle used but invalid pages

- Wear-Leveling
 - Each block has a limited lifetime in erasing counts

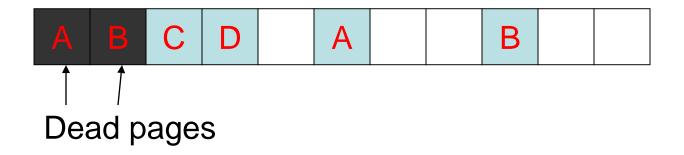
Page Write and Block Erase



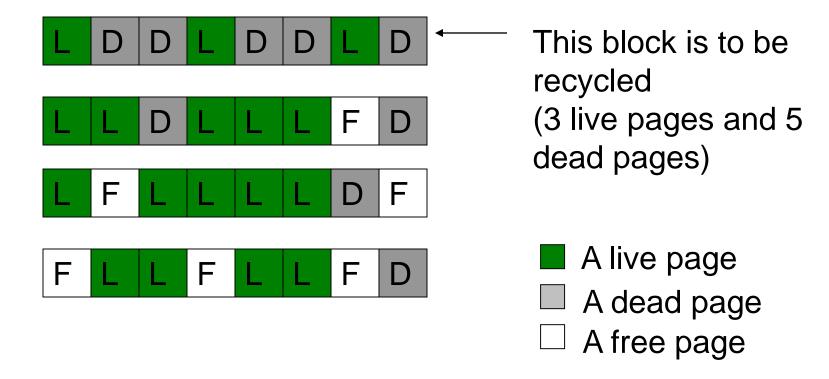
Out-Place Update



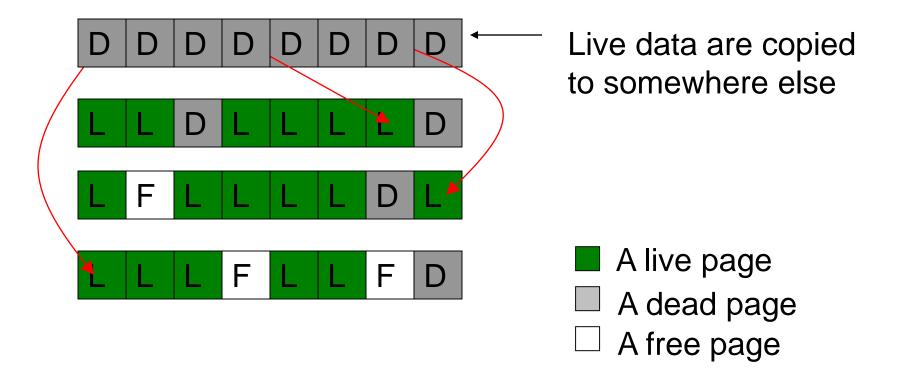
Suppose that we want to update data A and B...



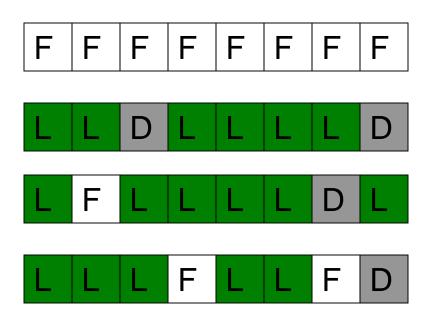
Garbage Collection (1/3)



Garbage Collection (2/3)



Garbage Collection (3/3)

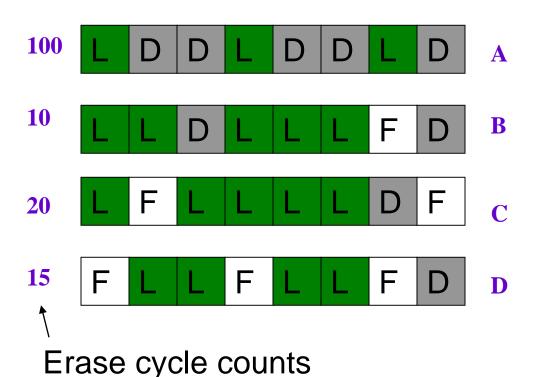


The block is then erased

Overheads:

- live data copying
- block erasing
 - A live page
 - A dead page
 - □ A free page

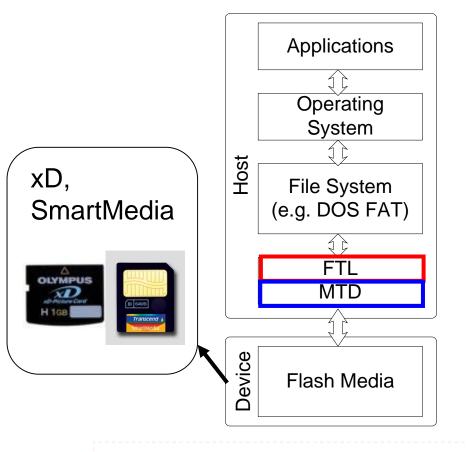
Wear-Leveling

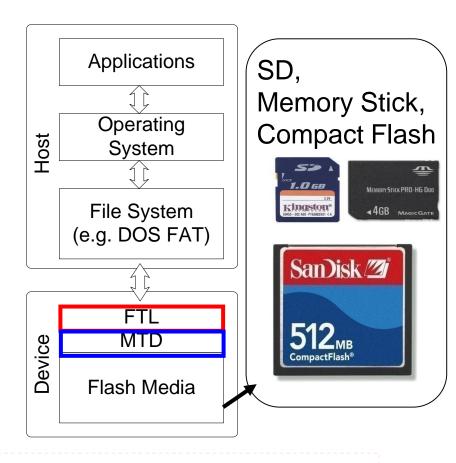


Wear-leveling might interfere with the decisions of the block-recycling policy

- A live page
- A dead page
- □ A free page

Flash Translation Layer

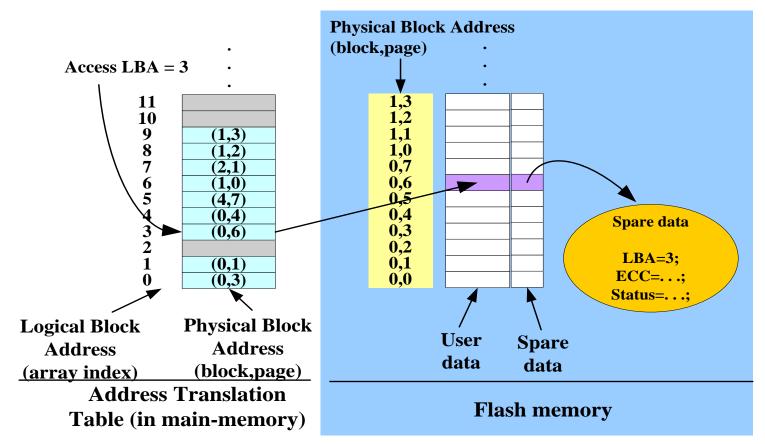




*FTL: Flash Translation Layer, MTD: Memory Technology Device

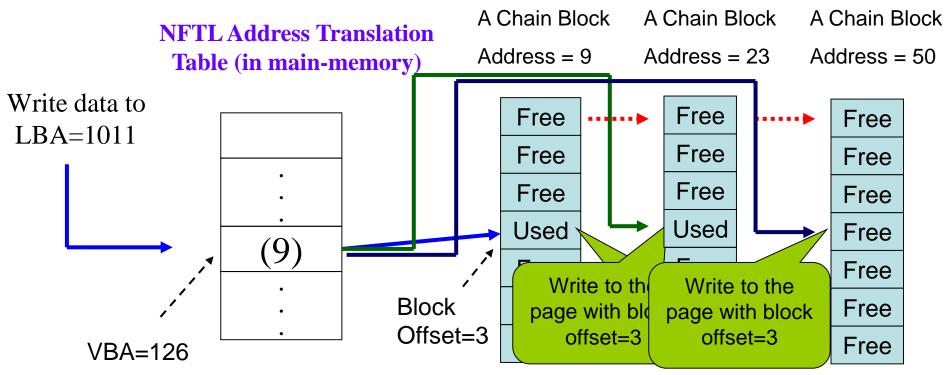
Policies - FTL

▶ FTL adopts a page-level address translation mechanism



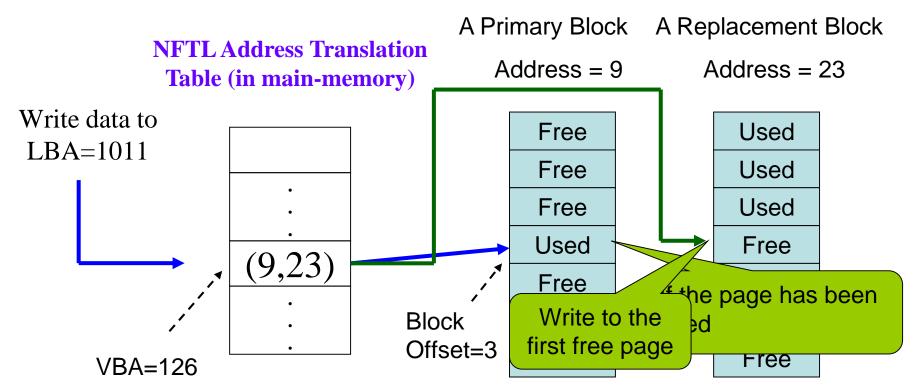
Policies - NFTL (Type 1)

A logical address under NFTL is divided into a virtual block address and a block offset, e.g., LBA=1011 => virtual block address (VBA) = 1011 / 8 = 126 and block offset = 1011 % 8 = 3



Policies – NFTL (Type 2)

A logical address under NFTL is divided into a virtual block address and a block offset, e.g., LBA=1011 => virtual block address (VBA) = 1011 / 8 = 126 and block offset = 1011 % 8 = 3



Challenges and Research Topics of Flash Memory Designs

Performance

- Reduce the overheads of Flash management
- Reduce the access time to data
- Reduce the garbage collection time

Reliability

- Error correcting codes
- Log systems

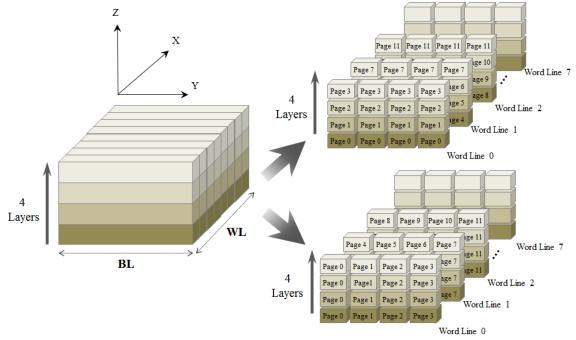
Endurance

- Dynamic wear-leveling
- Static wear-leveling



3D Flash Memory

- ▶ 3D flash memory provides a good chance to further scale down the feature size and to reduce the bit cost.
 - Deliver very large storage space
 - Worsen program disturbance



Deteriorated Disturb on 3D Flash

